MACOM GaN Reliability Presentation

GaN on Silicon Processes and Products
MACOM GaN on Silicon Reliability Presentation
MACOM GaN Strategy

**GaN on Silicon Carbide**
- 0.5µm GaN HEMT process
- 0.25µm GaN HEMT process
- Dual wafer foundries
- Reliable plastic packaging

**GaN on Silicon**
- Silicon cost structure
- 0.5µm GaN HEMT process
- 0.25µm GaN HEMT in 2014
- Reliable plastic packaging
- Epitaxial 8” agreement

**Largest GaN Solutions Portfolio Worldwide**
Substrate Comparison

- Thermal rise of 2mm FET (20x100um fingers) vs. substrate conductivity
- SiC is < 5% better

There is virtually no difference in thermal rise between thin silicon substrates and more exotic substrates.
Ex: Thermal Analysis of 100W GaN Devices

<table>
<thead>
<tr>
<th>Material</th>
<th>Thickness</th>
<th>R&lt;sub&gt;TH&lt;/sub&gt; (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN</td>
<td>2um</td>
<td>0.22°C/W</td>
</tr>
<tr>
<td>Si</td>
<td>150um</td>
<td>0.77°C/W</td>
</tr>
<tr>
<td>Au/Si</td>
<td>4um</td>
<td>0.02°C/W</td>
</tr>
<tr>
<td>CuW Package</td>
<td>1.5mm</td>
<td>0.8°C/W</td>
</tr>
</tbody>
</table>

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<thead>
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<th>Material</th>
<th>Thickness</th>
<th>R&lt;sub&gt;TH&lt;/sub&gt; (°C/W)</th>
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</thead>
<tbody>
<tr>
<td>GaN</td>
<td>2um</td>
<td>0.22°C/W</td>
</tr>
<tr>
<td>Si</td>
<td>50um</td>
<td>0.52°C/W</td>
</tr>
<tr>
<td>Au/Sn</td>
<td>4um</td>
<td>0.02°C/W</td>
</tr>
<tr>
<td>Cu Package</td>
<td>1.5mm</td>
<td>0.62°C/W</td>
</tr>
</tbody>
</table>

NPT25100, Gen 1  
R<sub>TH</sub> = 1.8°C/W

NPT1010, Gen 2  
R<sub>TH</sub> = 1.4°C/W

150μm to 50μm die thickness = 25% Improvement
CuW to pure Cu package = 24% Improvement

Many contributors to total thermal impedance
Substrate contribution is only about 1/3 of total
Measure $R_{TH}$ on Every Product Design

**NPT25100**

- $R_{JC} = 1.8 \, ^{\circ}C/W$

**NPT1010**

- $R_{JC} \sim 1.4 \, ^{\circ}C/W$

**DC Thermal Imaging:**

- $V_{DS} = 28V$, $I_D = 600mA$
- $P_{DISS} = 16.8W$
Process Qualification
Process Qualification Philosophy

• Determine Dominant EOL Failure Mechanism
  – Diffusion based failure mechanism
    • Wearout mechanism
    • Characterized by change in $I_{DS}$
  – Temperature accelerated life test
    • 3 temperature ALT
    • Step stress determined ALT junction temperatures
    • Design test for reasonable mean time to failure at each temperature
  – Perform
    • New or changed design process, e.g. transistor structure
    • New or changed fabrication process
Breakdown Voltage

• LDMOS and GaAs FETs have “avalanche breakdown”
  – VDS above this breakdown voltage can destroy the device
• Nitronex GaN devices do not have a breakdown like this
  – Nitronex specifies “breakdown” by measuring drain current leakage

![Graph showing drain leakage current (Id) at different drain voltages (Vds).](image)

- 9 devices tested from 3 wafers
- Very low leakage current up to 150V
  - 100W device -> 3mA leakage

Figure 1. Id (drain leakage) at $V_{GS} = -8$ and $V_{DS}$ from 0-150V
Process Reliability 0.5um GaN HEMT 28V
Accelerated Life Test

- Test device used is 4x100μm
- Dies selected from 3 process lots, >22 per temperature
- Biased at 28V and 70 – 90 mA/mm to achieve desired $T_J$ in oven
- Failure criterion is change of 20% in $I_{DS}$
- $T_J$ verified by QFI IR scan

MTTF of 1 million hrs at $T_J$ of 200°C and $E_a$ 2.2eV
Enhanced Breakdown Voltage

Gate-Drain Spacing 2 microns | Gate-Drain Spacing 3 microns | Gate-Drain Spacing 4 microns

GD2 | GD3 | GD4

28V Technology | 48V Technology

• BV Testing shows expected trend of increasing BV with GD spacing (~50-80V/µm).

Achieved >200V breakdown voltage for 48V NRF2 Technology
Process Reliability 0.5um GaN HEMT 48V
Accelerated Life Test

- Test device used is 4x100µm
- Dies selected from 3 process lots, >22 per temperature
- Biased at 48V and 40 – 52.5mA/mm to achieve desired $T_J$ in oven
- Failure criterion is change of 20% in $I_{DS}$
- $T_J$ verified by QFI IR scan

*$MTTF$ of 1 million hrs at $T_J$ of 200°C and $E_a$ 2.2eV*
Product Qualification
Product Reliability

• FMEA Qualification of Packaged Product
  – Identify all potential failure modes for packaged GaN die
  – Determine responsible failure mechanism(s)
  – Determine stress test to verify robustness against failure mechanism

<table>
<thead>
<tr>
<th>Potential Failure Mode</th>
<th>Potential Failure Mechanism</th>
<th>Test to Stress Potential Failure Mechanism</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die cracking</td>
<td>CTE mismatch molding compound to die</td>
<td>Temperature cycling -65C to 150C</td>
<td>PASS</td>
</tr>
<tr>
<td>Delamination of molding compound</td>
<td>Reflow</td>
<td>MSL testing + reflow simulation</td>
<td>PASS</td>
</tr>
</tbody>
</table>

Goal: stress all potential failure mechanisms to ensure that you don’t “fall off” the process reliability Arrhenius curve.
Product Qualification Methodology

• Product level potential failure mechanism sources
  – Assembly processes (wirebond, die attach, …)
  – Package integrity (moisture, temp cycling, …)

• When is Qualification Performed?
  – New or changed design process, e.g. transistor structure
  – New or changed fabrication process
  – New or changed package assembly process or vendor
  – Periodic ongoing reliability monitoring
### Qualification Test Results (typ.)

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Test Standard</th>
<th>Sample Set</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-Temp DC</td>
<td>JEP118-B</td>
<td>30 Devices/Temp @ 260, 285, and 310°C</td>
<td>Ea = 2.0 eV, MMF &gt; 10^7 hours at 150°C</td>
</tr>
<tr>
<td>DC-HTOL</td>
<td>JESD22-A108</td>
<td>45 devices, 2000 hours</td>
<td>20-yr Imax drift &lt;7% at 200°C 20-yr Imax drift &lt;3% at 150°C</td>
</tr>
<tr>
<td>RF-HTOL</td>
<td>JESD22-A101-A</td>
<td>12 Devices, 500 hours</td>
<td>&lt; 0.25 dB drift through 500 hours</td>
</tr>
<tr>
<td>ESD-HBM</td>
<td>JESD22-A114</td>
<td>9</td>
<td>&gt;1000V (class 1C) for NPT35050</td>
</tr>
<tr>
<td>ESD-MM</td>
<td>JESD22-A115</td>
<td>9</td>
<td>&gt;200V (class M3) for NPT35050</td>
</tr>
<tr>
<td>Thermal Impedance</td>
<td>IR imaging</td>
<td>9</td>
<td>All samples meet datasheet target of 1.95°C•/mW for NPT35050</td>
</tr>
<tr>
<td>Autoclave</td>
<td>JESD22-A102</td>
<td>45</td>
<td>Minimal change in performance</td>
</tr>
<tr>
<td>VSWR</td>
<td>10:1 VSWR</td>
<td>5</td>
<td>Minimal change in performance</td>
</tr>
<tr>
<td>Temp. Cycling</td>
<td>JESD22-A104</td>
<td>45</td>
<td>Minimal change in performance</td>
</tr>
<tr>
<td>Thermal Shock</td>
<td>M-750-1056</td>
<td>15</td>
<td>Minimal change in performance</td>
</tr>
<tr>
<td>Solderability</td>
<td>JESD22-B102</td>
<td>4</td>
<td>Passed</td>
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<tr>
<td>Mech. Shock</td>
<td>M-883-2002</td>
<td>38</td>
<td>Passed</td>
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<tr>
<td>Vibration</td>
<td>M-883-2007</td>
<td>38</td>
<td>Passed</td>
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<tr>
<td>Const. Acceleration</td>
<td>M-883-2001</td>
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<td>Passed</td>
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<tr>
<td>Moisture Res.</td>
<td>M-883-1004</td>
<td>38</td>
<td>Passed</td>
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<tr>
<td>Salt Atmosphere</td>
<td>M-883-1009</td>
<td>15</td>
<td>Passed</td>
</tr>
<tr>
<td>Solvent Res.</td>
<td>M-883-2015</td>
<td>15</td>
<td>Passed</td>
</tr>
<tr>
<td>Bond Strength</td>
<td>M-750-2037</td>
<td>15</td>
<td>Passed</td>
</tr>
</tbody>
</table>

- Demonstrated reliability, combined with superior RF performance, qualifies Nitronex as a leading RF device supplier.
- Qualification plan follows JEDEC and MIL Standards.
- List of tests typical of LDMOS or RF power device qualification reports.
Qualification Test Results

28V and 48V Product Accumulate Equivalent Device Hours

**28V**
\[ T_J = 180^\circ C, \ 200^\circ C \]
2.5 Million Equivalent Device Hours

**48V**
\[ T_J = 200^\circ C, \ 225^\circ C \]
14.5 Million Equivalent Device Hours
NPT2022 Thermal Resistance Method

- $R_{JC} = 1.3 \text{ C/W (48V)} @ 225 \, T_J$
  - Important to determine $R_{th}$ at high temp
  - $R_{th}$ determined using 3um

- Same IR method used for accelerated life test junction temperature determination
Reliability at Operating Temperatures
Plastic Package HTOL (<25W)

System Description
- 4 systems, 32 DUTs per system
- Hot plate with chiller temperature controlled to +/-1°C

HTOL Rack
Hotplate with burn-in board

- Constant $I_{DS}$ system, software controlled
- Constant in-situ monitoring of $V_{DS}$, $V_{GS}$, $I_{GS}$, $I_{DS}$
- T0 (initial) tests and periodic down point testing performed in-situ
- Testing includes both DC and RF msmts

RF Test Rack
High Power HTOL (25 to 200W)

- Constant $V_{GS}$ system
- $I_{DS}$ maintained by periodic manual biasing of devices
- Baseplate temperature maintained via external chiller
- Constant in-situ monitoring of $V_{DS}$, $V_{GS}$, $I_{GS}$, $I_{DS}$
- T0 (initial) tests and periodic down point testing performed at ATE

High Power HTOL

- 50 devices per side, 100 total
- 200W max dissipation per DUT
NPT1015 VSWR Robustness Testing

- 3 devices subjected to 10:1 and 20:1 output VSWR mismatch
- Freq: 3.0GHz, \( V_{DS}=28V \), Run at \( P_{SAT} \) (50W) @ 90°C
- Phase rotated from 0° to 360° in 5° steps over 120 seconds → ~1.6s/phase angle
- Maximum \( T_J \) peak >300°C during test

- Devices exhibited minimal shift
  - < 1dB change in gain
  - 0.3dB change in \( P_{SAT} \)
  - 2 point change in efficiency
  - No further degradation with repeated test

- See application note AN-004 for more details
GaN on Silicon Field Reliability

• 1 million devices fielded
  – MIL radios and EW
  – CATV
  – Infrastructure

• High volume software defined military radio program
  – 6 years of volume production
  – Harsh environmental conditions
  – No field returns to date
GaN Reliability in Your Product
Recommendations for GaN Devices

• Use Well Designed Bias Circuits
  – Sequence RF, Gate, and Drain Voltages
    • See application notes
  – Avoid glitches, stray RF, that could cause $V_{GS}$ to fail
    • Charge pump inverters and op-amps are EMI susceptible
  – Monitor gate current
    • High $I_G$ indicates severe overdrive
  – Bias/decoupling components
    • Affect risetime, falltime, IM performance, memory effects
    • Review transient, modulation BW, RF frequency effects
    • Wideband amplifiers present special challenges
      – Gate/drain bias chokes subject to resonances
      – Look for narrowband loss of efficiency and power
      – Add resistors, networks to lower or control Q
Stability Considerations

- Low Frequency Stability
  - RF transistors have enormous LF gain
  - Open (high Z) input = DANGER
  - Gate resistor tames LF loop gain
  - Large caps at $V_{\text{GATE}}$ and $V_{\text{DRAIN}}$
    - Improves stability
    - Critical for linearity, intermod, ACPR

- Low Frequency Equivalent Circuit
  - Gate sees 50 ohms to ground
  - Verify stability w/ CAD tools
  - Sweep both model and circuit
Recommendations for GaN Devices

- **Controlled** $T_J$ = Good Reliability
  - Consider the entire thermal path from device to heatsink
  - SMT Plastic Packages
    - Use recommended via pattern
    - Void free solder attach
    - Know the board thermal $Z$
    - PCB backside attach to heatsink
  - TO-272 Plastic Power Package
    - Solder attach preferred
    - Use “Clamping Device” to keep contact on flange center
  - VSWR
    - High VSWR can increase $T_J$
    - Include VSWR monitoring and protection
  - Understand the Operating Conditions
    - What is the actual power and efficiency?
    - What are the actual conditions in the end product?
Good PCB Thermal Attach

Screws lower PCB-to-Heatsink thermal resistance

4x4 QFN
NPTB00025 VSWR Phase Sweep, T ~ 25°C

- A high junction temperature is reached (250°C) is reached
- A high gate current is observed out-of-phase to maximum temperature
- A rugged device withstands high voltages at ~100°C channel temperature
Thermal Budgeting

• **Typical Thermal Budget**
  – NPT2022 48V@100W  $R_{TH} = 1.3^\circ C/W$
  – “100W” is “rated power” in a narrowband test circuit
     • Most vendors use the same ratings
  – Broadband power will be lower
     • Depends on bandwidth and matching circuit
     • How close to $Z_{OPT}$?
  – Ex: 100-1000 MHz Broadband Amplifier
     • Delivers 80W @ 50% worst case efficiency
     • $P_{DISS} = 80W$ (DC) + 5W ($P_{IN}$)
     • $T_{RISE} = 85W * 1.3^\circ C/W = 111^\circ C$
     • Max $T_{FLANGE} = 89^\circ C$ for $T_{J} = 200^\circ C$

This design has good thermal margin