UltraCMOS® RF Power Limiters, the CMOS Monolithic Alternative to Discrete, Pin-diode Limiters
Peregrine: Solving the World’s Toughest RF Challenges

Fabless semiconductor company

- Pioneered use of CMOS SOI for RF
- Performance on par with GaAs, with all the benefits of CMOS
- Perfected technology over 25 years

Serving multiple end-markets

- Leading innovator in the mobile handset space
- Bringing RF innovation to aerospace, automotive test & measurement and other industrial markets
- Initial Public Offering August 2012
- Headquarters in San Diego, CA
- 300+ employees
Limiting power into electronic devices is needed for various markets and applications spanning Test & Measurement, WI, LMR, and RADAR.

- Protecting the RF ports in test & measurement equipment from unexpected power surges
- Protecting the RF Front End/LNAs in communications modules
- Protecting receivers in tactical radios from intentional jammers in military warfare
- Protecting TRX modules in RADAR systems
- Protection of electronic components from ESD strikes
Ideal Power Limiter

- Below a threshold (P1dB) level the limiter passes the input signal to the output without attenuation.
- At the threshold the limiter “limits” the amount of input power that is passed to the output, up to the max power.
- The “Limiting Range” is the power range between the threshold and max power level.
- At max power the amount of signal that “leaks” to the output is specified as the leakage power.
Power Limiter Product Considerations

- PCB Area / Footprint
- Thermal / Heat Dissipation
- RF Performance
  - Ins Loss / Isolation
  - IIP3 / IIP2
  - Leakage Power
  - P1dB / Limiting Threshold
- Response / Recovery Time
- ESD Rating & Protection

- Ease of Design In
- Eng Dev Costs
- Bill of Materials (BOM)
- Flexibility
- Repeatability
- Reliability

Power Limiter product objectives can be achieved with the right process technology choice
PIN Diode – The Limiter Building Block

- PIN diodes have been solution of choice for decades
- PIN diodes have a lightly doped intrinsic “I” layer between the two more heavily doped “P” and “N” layers
- The intrinsic “I” region permits the diode to act as a current-controlled resistor that can switch between a high-Z state and a low-Z state
- The PIN junction capacitance affects the amount of signal that will be allowed to pass through the device when it is in the high-Z “Off” state
- PIN diodes can be manufactured in GaAs or Silicon
Discrete PIN diode limiters are commonly used to accomplish the power limiting function.

**Advantages:**
- Low small-signal Insertion loss
- High maximum power handling
- Stand alone device, no detector or control loop needed

**Disadvantages:**
- Requires bias inductor & DC blocking caps
- Slow response and recovery time
- Poor linearity
- Limited Integration with other functional blocks
- Low ESD rating
UltraCMOS® Technology – A Monolithic Alternative

• UltraCMOS® is a patented variation of Silicon-On-Insulator (SOI) technology
  • Thin-film silicon is processed on a semi-insulating substrate
  • The substrate can be either Sapphire or Silicon

• The “CMOS” in UltraCMOS signifies that standard CMOS manufacturing processes are used in the device fabrication
  • Most widely used semiconductor process technology in the world
  • Known for reliability, high yield, low cost, and monolithic integration

• A high resistivity substrate minimizes substrate loss and parasitic capacitance
  • Critical for minimizing insertion loss and maximizing bandwidth and isolation
  • Reduces dissipated power and simplifies thermal management
Monolithic Integration of RF, Analog and Digital

32W SP5T Switch
4Tx + 1Rx RF Paths

- **Integrated Bias, Control Logic & ESD**
  - No external biasing components
  - Industry leading ESD rating

- **Reliable and Optimal Performance**
  - Reduces variations due to external application circuit

- **Ease of Use**
  - Simple control through on-board control interfaces
  - Simple applications circuit

- **Small Form Factor**
  - 5x5 mm QFN package
UltraCMOS® Power Limiter Concept

Peregrine’s UltraCMOS monolithic power limiters integrate RF, analog, and digital functions to maximize performance, flexibility, and reliability.

- Normal Linear Power Limiting
  - Below P1dB, limiter is “invisible” to the load, featuring exceptional RF performance.
  - At P1dB, the limiter starts to limit the input power, up to Pmax.

- Adjustable Limiting Threshold
  - An external control voltage can be used to tradeoff P1dB, leakage power, and linearity.

- Extreme Power Reflecting Mode
  - Incident power is reflected back to source

- Unbiased protection up to Pmax

- NO external biasing inductors, resistors, or blocking capacitors are required!
PIN Diode Limiter implementation requires:
- Quarter-Wavelength Transmission Line
- Bias Inductor
- DC Blocking Capacitors
- External ESD Protection
- PCB Area!
Smaller, monolithic device begs the question - How much power can such a device safely dissipate without overheating?

- UltraCMOS limiters can safely dissipate 5W of power with +40dBm CW applied
  - No external heat sinks needed
  - No thick Copper layers needed on PCB
  - Thermal resistance is ~16 °C/W

- With PIN diodes some RF power is dissipated in the diode, requiring careful management of heat
  - Thermal resistance of packaged PIN diodes is high, increasing the junction temperature and exponentially reducing the device lifetime ~ 80 °C/W
UltraCMOS power limiters deliver exceptional small-signal and large-signal RF performance in a small footprint.

Low, wideband Insertion Loss: 
< 1dB up to 6GHz

Return Loss stable over temp: 
> 30dB @ 6GHz
UltraCMOS power limiters deliver exceptional small-signal and large-signal RF performance in a small footprint.

Adjustable P1dB: +22dBm to +32dBm

Exceptional linearity over temp:
~65dBm IIP3
~105dBm IIP2
Power limiters are required not only to instantaneously respond to large signals but recover quickly from the limiting event.

- Recovery time in PIN diodes depends on the minority carrier lifetime (volume and resistivity of the “I” layer) \( \sim 10^{\text{s of ns}} \)

- No single cycle slipped
- Both response & recovery time is \(< 1\text{ns}\)
Since DC blocking capacitors are not required, an UltraCMOS limiter can be used as an ESD clamp to protect the RF ports from ESD strikes.

- SOI open drain devices protect themselves from ESD strikes
  - HBM Class 3A (8kV) rating

- Given a 2kV HBM ESD strike, UltraCMOS limiter can clamp the output voltage to different levels based on external Vctrl setting

- PIN diodes have ESD ratings several orders of magnitude worse, especially if designed in GaAs
  - HBM Class 0 (250V) rating
Peregrine’s UltraCMOS Power Limiter Solutions

Low Threshold

PE45140

- 20MHz to 2GHz frequency support
- High power handling of 50W
- Adjustable limiting threshold from +22dBm to +32dBm
- Fast response time of < 1ns
- Leakage power of +30dBm
- Dual-mode operation
- Unbiased power limiting operation
- Max IIP3 of +64dBm
- Low insertion loss of 0.6dB @ 2GHz
- ESD rating of 8KV HBM

Wide Bandwidth

PE45450

- 9KHz to 6GHz frequency support
- High power handling of 50W
- Adjustable limiting threshold from +25dBm to +35dBm
- Fast response time of < 1ns
- Leakage power of +33dBm
- Dual-mode operation
- Unbiased power limiting operation
- Max IIP3 of +70dBm
- Low insertion loss of 0.8dB @ 6GHz
- ESD rating of 8KV HBM
PE45140 & PE45450 deliver simple, repeatable, and reliable protection for demanding professional mobile/portable radios and T&M applications.

**Power Handling**
- 50W pulsed enables receiver designs to handle large jammers and unexpected power surges

**Adjustable P1dB**
- Adjustable limiting threshold enables flexible power limiting across different platforms and architectures

**Fast Response Time**
- <1ns ensures instantaneous protection of sensitive components and rapid return to normal operation

**Exceptional ESD**
- 8kV HBM a key benefit for demanding and harsh environments that require high ESD ratings
Software Defined Tactical Radios used in military communications require a power limiter to protect the Receiver from intentional jammers.

- **High Power Handling**
- **Fast Response & Recovery Time**
Test Equipment use power limiters to protect RF ports from unexpected power surges.

- **Excellent ESD Protection**
- **High Linearity**
Datasheets posted to [www.psemi.com](http://www.psemi.com)

Samples and EVK’s available today
UltraCMOS® Power Limiter Roadmap

Today

PE45450
9K-6GHz
50W
25-35dBm
Threshold

PE45140
20M-2GHz
50W
22-32dBm
Threshold

Tomorrow

30GHz Power Limiter

100W Power Limiter

10dBm Threshold Power Limiter

Power Detector + Limiter

Higher Frequency

Higher Power

Lower Threshold

More Features
# The UltraCMOS® Advantage

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<th>PIN Diode Limiter</th>
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<td>Eliminates external biasing components</td>
<td>✓✓✓</td>
<td>✗</td>
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<tr>
<td>Superior ESD ratings</td>
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<tr>
<td>Protection in unpowered conditions</td>
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In Conclusion: CMOS Power Limiters Have Arrived

• Peregrine Semiconductor is the inventor of RF-SOI
  • UltraCMOS is a patented variation of SOI
  • High resistivity substrate is key enabler

• UltraCMOS is a viable technology alternative to GaAs based PIN diode power limiters
  • 50W designs available today, more products to follow

• UltraCMOS Power Limiters are monolithic solutions bringing fundamental improvements in 3 key areas:
  • RF Performance
  • Product Reliability
  • Monolithic Integration